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Applicant: Kunihiro MIMA, et al. : Art Unit:
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FOR: METHOD FOR DRIVING PLASMA DISPLAY PANEL

VERIFICATION OF A TRANSLATION

Assistant Commissioner for Patents
Washington, D.C. 20231
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I, the below named translator, hereby declare that:

1. My name and post office address are as stated below.
2. That I am knowledgeable in the English language and in the language of JP2004-152802, and I believe the attached English translation to be a true and complete translation of JP2004-152802.
3. The document for which the attached English translation is being submitted is a patent application on an invention entitled METHOD FOR DRIVING PLASMA DISPLAY PANEL.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: December 3, 2008

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[NAME OF ARTICLE] Specification 1

[NAME OF ARTICLE] Drawing 1

[NAME OF ARTICLE] Abstract 1

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[Claim 1]

A method for driving a plasma display panel having an initialization period in which a discharge cell is formed at an intersection between a scan electrode and a sustain electrode, and initializing discharge is generated in the discharge cell, a writing period in which writing discharge is generated in the discharge cell, and a sustain period in which sustain discharge is generated by alternately applying sustain pulses to the scan electrode and the sustain electrode of the discharge cell, wherein the rise time of the sustain pulse applied to the scan electrode and the sustain electrode during the sustain period is shortened on a cycle of once every plurality of times.

[Claim 2]

A method for driving a plasma display panel wherein the rise time of a sustain pulse applied to a scan electrode and a sustain electrode during a sustain period is shortened on a cycle of at least once every three times.

[Name of the Document] Specification

[Title of the Invention] Method of driving plasma display panel

[Field of the Invention]

[0001]

The present invention relates to a method for driving a plasma display panel.

[Background Art]

[0002]

In a surface discharge AC type panel that is typical as a plasma display panel (hereinafter referred to as panel), many discharge cells are formed between a front panel and a rear panel which are disposed opposite to each other. On the front panel, two or more pairs of display electrodes formed of a pair of scan electrode and sustain electrode are formed in parallel to each other on a front glass substrate, and a dielectric layer and a protective layer are formed in such manner as to cover the display electrodes. On the rear panel, a plurality of parallel data electrodes are formed on a rear glass substrate, and a dielectric layer is formed so as to cover the data electrodes. In addition, a plurality of partitions are formed thereon in parallel fashion with the data electrodes, and a phosphor layer is formed on the surface of the dielectric layer and the side surface of the partition. And, the front panel and the rear panel are disposed opposite to each other and sealed so that the display electrode and the data electrode are positioned in a two-level crossing fashion, and a discharge gas is filled into the internal discharge space. A discharge cell is formed at a portion where the display electrode is opposed to the data electrode. In a panel

having such a configuration, ultraviolet ray is generated by gas discharge in each discharge cell, and the ultraviolet ray excites the phosphor of each of RGB colors and lets it emit light to make color display.

[0003]

As a method for driving a panel, a sub-field method is generally employed. In the method, one-field period is divided into a plurality of sub-fields and gradation display is performed by combining the sub-fields activated for light emission. Also, among the sub-field methods, a novel driving method in which light emission not related to gradation expression is reduced as much as possible to improve the contrast ratio is disclosed in Patent document 1.

[0004]

The sub-field method will be briefly described in the following. Each sub-field includes an initialization period, a writing period, and a sustain period. First, in the initialization period, initializing discharge is simultaneously performed in all the discharge cells, thereby erasing the hysteresis of wall charge to the earlier individual discharge cells and forming necessary wall charge for the subsequent writing operation. In addition, it has a function of generating priming (initiator = exciting particle for discharge) for lessening the delay in discharge and stabilizing the generation of writing discharge. In the subsequent writing period, scan pulses are sequentially applied to the scan electrode and also writing pulses corresponding to the image signal to be displayed are applied to the data electrode, and thereby, writing discharge is selectively generated between the scan electrode and data electrode, selectively forming the wall charge.

In the sustain period, a predetermined number of sustain pulses in accordance with the brightness weight are alternately applied between the scan electrode and sustain electrode, and thereby, the discharge cells with wall charge formed by writing discharge are selectively discharged for light emission.

[Patent document 1] Unexamined Japanese Patent Publication 2002-351396.

[Disclosure of the Invention]

[Problems to be Solved by the Invention]

[0005]

In the case of a panel having such a structure, there has been a problem such that the generation timing of discharge varies every discharge cell due to the display conditions, and consequently, the light emission intensity varies every discharge cell, and the brightness of light emitted becomes non-uniform in some regions as a whole of the screen.

[0006]

The present invention is intended to solve the problems, and the object of the invention is to prevent the display quality from becoming lowered due to generation of regions being non-uniform in brightness without increase of the power consumed.

[Means to Solve the Problems]

[0007]

The method for driving a plasma display of the present invention is a plasma display panel driving method having an initialization period in which a discharge cell is formed at an intersection between a scan electrode

and a sustain electrode, and initializing discharge is generated in the discharge cell, a writing period in which writing discharge is generated in the discharge cell, and a sustain period in which sustain discharge is generated by alternately applying sustain pulses to the scan electrode and the sustain electrode of the discharge cell, wherein the rise time of the sustain pulse applied to the scan electrode and the sustain electrode during the sustain period is shortened on a cycle of once every plurality of times.

[0008]

Also, in the present invention, the rise time of the sustain pulse applied to the scan electrode and sustain electrode during the sustain period is shortened on a cycle of once every three times at least.

[Advantages of the Invention]

[0009]

According to the present invention, the generation of regions where the brightness of emitted light becomes non-uniform can be reduced as a whole of the screen, and in addition, it can be realized without changing the sustain pulse voltage or pulse width and it is possible to suppress the increase of the power consumed.

[Preferred Embodiments for Carrying Out the Invention]

[0010]

The method for driving a plasma display panel in one preferred embodiment of the present invention will be described in the following with reference to the drawings.

[0011]

Fig. 1 is a perspective view showing an essential portion of a panel

used for one preferred embodiment of the present invention. Panel 1 is configured in that front substrate 2 and rear substrate 3 made of glass are disposed opposite to each other, and a discharge space is formed between the panels. A plurality of scan electrodes 4 and sustain electrodes 5 configuring the display electrode are formed in paired and parallel fashion on front panel 2. And, dielectric layer 6 is formed so as to cover scan electrode 4 and sustain electrode 5, and protective layer 7 is formed on dielectric layer 6. Also, a plurality of data electrodes 9 covered with insulator layer 8 are disposed on rear substrate 3, and partition 10 is disposed in parallel to data electrode 9 on insulator layer 8 between data electrodes 9. Also, phosphor 11 is disposed on the surface of insulator layer 8 and on the side of partition 10. And, front panel 2 and rear panel 3 are disposed opposite to each other in the direction of intersections of scan electrode 4, sustain electrode 5 and data electrode 9, and a mixed gas of neon and xenon as a discharge gas for example is filled in the discharge space formed therebetween.

[0012]

Fig. 2 is an electrode layout of a panel in one preferred embodiment of the present invention. In the direction of the lines, n pieces of scan electrodes SCN1 to SCN n (scan electrode 4 in Fig. 1) and n pieces of sustain electrodes SUS1 to SUS n (sustain electrode 5 in Fig. 1) are alternately arranged. In the direction of the rows, m pieces of data electrodes D1 to D m (data electrode 9 in Fig. 1) and are arranged. And, a discharge cell is formed at a portion where a pair of scan electrode SCN i and sustain electrode SUS i ($i = 1$ to n) intersect one data electrode D j ($j = 1$ to m), and m

x n pieces of discharge cells are formed in the discharge space.

[0013]

Fig. 3 is a structural diagram of a plasma display device using the panel driving method in a preferred embodiment of the present invention. The plasma display device comprises panel 1, data electrode drive circuit 12, scan electrode drive circuit 13, sustain electrode drive circuit 14, timing generator circuit 15, AD (analog to digital) converter 18, scanning line conversion section 19, sub-field conversion section 20, and a power supply circuit (not shown).

[0014]

In Fig. 3, video signal VD is inputted to AD converter 18. Also, horizontal synchronizing signal H and vertical synchronizing signal V are applied to timing generator circuit 15, AD converter 18, scanning line conversion section 19, and sub-field conversion section 20. AD converter 18 converts video signal VD into picture data in the form of digital signal and gives the picture data to scanning line conversion section 19. Scanning line conversion section 19 converts the picture data into picture data corresponding to the number of pixels of panel 1, and gives the data to sub-field conversion section 20. Sub-field conversion section 20 divides the picture data of each pixel into a plurality of bits corresponding to a plurality of sub-fields, and outputs the picture data every sub-field to data electrode drive circuit 12. Data electrode drive circuit 12 converts the picture data every sub-field into signal corresponding to each data electrode D1 to Dm and drives each data electrode.

[0015]

Timing generator circuit 15 generates timing signal on the basis of horizontal synchronizing signal H and vertical synchronizing signal V, and gives the signal to each scan electrode drive circuit 13 and sustain electrode drive circuit 14. Scan electrode drive circuit 13 supplies driving voltage wave-form to scan electrodes SCN1 to SCNn on the basis of the timing signal, and sustain electrode drive circuit 14 supplies driving voltage wave-form to sustain electrodes SUS1 to SUSn on the basis of the timing signal.

[0016]

The driving voltage wave-form for driving the panel and its operation will be described in the following.

[0017]

Fig. 4 is a wave-form chart of voltage applied to each electrode of the plasma display panel in the preferred embodiment of the present invention, and in the chart, driving voltage wave-forms are shown with respect to a sub-field having an initialization period for executing the initialization of all cells (hereinafter referred to as all cell initialization sub-field) and a sub-field having an initialization period for executing selective initialization (hereinafter referred to as selective initialization sub-field).

[0018]

First, the driving voltage wave-form of all cell initialization sub-field and its operation is described. In Fig. 4, in the initialization period, data electrodes D1 to Dm and sustain electrodes SUS1 to SUSn are maintained at 0 (V), and a ramp voltage gradually increasing from voltage Vp (V) lower than the discharge start voltage toward voltage Vr (V) higher than the

discharge start voltage is applied to scan electrodes SCN1 to SCNn. Then, the first weak initialization discharge takes place in all the discharge cells, and negative wall voltage is built up in scan electrodes SCN1 to SCNn, and also, positive wall voltage is built up in sustain electrodes SUS1 to SUSn and data electrodes D1 to Dm. In this case, wall voltage in electrodes is a voltage generated due to wall charge built up in the dielectric layer or phosphor layer covering the electrodes. After that, sustain electrodes SUS1 to SUSn are maintained at positive voltage V_h (V), and a ramp voltage gradually decreasing from voltage V_g (V) toward voltage V_a (V) is applied to scan electrodes SCN1 to SCNn. Then, the second weak initialization discharge takes place in all the discharge cells, and the wall voltage in scan electrodes SCN1 to SCNn and the wall voltage in sustain electrodes SUS1 to SUSn are weakened, and the wall voltage in data electrodes D1 to Dm is also adjusted to a level suited for writing operation. Thus, the initialization in all cell initialization sub-field is all cell initializing operation in which initialization discharge takes place in all discharge cells.

[0019]

In the subsequent writing period, as shown in Fig. 4, scan electrodes SCN1 to SCNn are once maintained at V_s (V). Next, out of data electrodes D1 to Dm, positive writing pulse voltage V_w (V) is applied to data electrode Dk of the discharge cell to be displayed on the first line, and also, scanning pulse voltage V_b (V) is applied to scan electrode SCN1 on the first line. In this case, the voltage at the intersection between data electrode Dk and scan electrode SCN1 is a voltage obtained by adding the wall voltage in data electrode Dk and the wall voltage in scan electrode SCN1 to externally

applied voltage ($V_w - V_b$), and it exceeds the discharge start voltage. And, writing discharge takes place between data electrode D_k and scan electrode $SCN1$ and between sustain electrode $SUS1$ and scan electrode $SCN1$, then positive wall voltage is built up in scan electrode $SCN1$ of the discharge cell, while negative wall voltage is built up in sustain electrode $SUS1$, and negative wall voltage is also built up in data electrode D_k . In this way, writing discharge takes place in the discharge cell to be displayed on the first line, thereby executing the writing operation for building up wall voltage in each electrode. On the other hand, the voltage at the intersection between the data electrode and scan electrode $SCN1$, to which positive writing pulse voltage V_w (V) is not applied, does not exceed the discharge start voltage, and therefore, no writing discharge is generated. The writing operation as described above is sequentially performed up to the discharge cell on the n -th line to finish the writing period.

[0020]

In the subsequent sustain period, as shown in Fig. 4, sustain electrodes $SUS1$ to $SUSn$ are first shifted back to 0 (V), and positive sustain pulse voltage V_m (V) is applied to scan electrodes $SCN1$ to $SCNn$. In the discharge cell where writing discharge takes place, the voltage between scan electrode $SCNi$ and sustain electrode $SUSi$ becomes a voltage that is equal to the level obtained by adding the wall voltages of scan electrode $SCNi$ and sustain electrode $SUSi$ to sustain pulse voltage V_m (V) and it exceeds the discharge start voltage. And, sustain discharge takes place between scan electrode $SCNi$ and sustain electrode $SUSi$, then negative wall voltage is built up in scan electrode $SCNi$, while positive wall voltage is built up in

sustain electrode SUS_i. In this case, positive wall voltage is also built up in data electrode D_k. In the discharge cell where no writing discharge takes place during the writing period, no sustain discharge is generated, maintaining the wall voltage condition at the end of initialization period. Subsequently, scan electrodes SUS1 to SUS_n are shifted back to 0 (V), and positive sustain pulse voltage V_m (V) is applied to sustain electrodes SUS1 to SUS_n.

[0021]

Then, in the discharge cell where sustain discharge takes place, the voltage between sustain electrode SUS_i and scan electrode SCN_i exceeds the discharge start voltage. Accordingly, sustain discharge again takes place between sustain electrode SUS_i and scan electrode SCN_i, then negative wall voltage is built up in sustain electrode SUS_i, and positive wall voltage is built up in scan electrode SCN_i. Similarly, sustain pulses are alternately applied to scan electrodes SCN1 to SCN_n and sustain electrodes SUS1 to SUS_n, and thereby, sustain discharge continuously takes place in the discharge cell where writing discharge is generated during the writing period. In the final stage of sustain period, so-called narrow pulses are applied between scan electrodes SCN1 to SCN_n and sustain electrodes SUS1 to SUS_n to eliminate the wall voltage of scan electrodes SCN1 to SCN_n and sustain electrodes SUS1 to SUS_n while leaving positive wall charge in data electrode D_k. In this way, the sustain operation in the sustain period is completed.

[0022]

The driving voltage wave-form in the selective initialization

sub-field and its operation is described in the following. In the selective initialization period, sustain electrodes SUS1 to SUSn are maintained at V_h (V), while data electrodes D1 to Dm are maintained at 0 (V), and a ramp voltage gradually decreasing from V_q (V) toward V_a (V) to scan electrodes SCN1 to SCNn. Then, in the discharge cell where sustain discharge is executed during the sustain period in the previous sub-field, weak initialization discharge takes place, weakening the wall voltage of scan electrode SCNi and sustain electrode SUSi, and the wall voltage of data electrode Dk is also adjusted to a value suited for writing operation. On the other hand, no discharge takes place in the discharge cell where no writing discharge and sustain discharge are executed in the previous sub-field, maintaining the wall charge condition at the end of initialization period of the previous sub-field. Thus, the initialization in the selective initialization sub-field is a selective initialization for initialization discharge in the discharge cell where sustain discharge is executed in the previous sub-field.

[0023]

As for the writing period and sustain period, light emission corresponding to the picture signal input can be executed by performing the same operation as in the writing period and sustain period of the above-mentioned all cell initialization sub-field.

[0024]

In the plasma display panel, the generation timing of discharge varies every discharge cell depending on the display condition, and consequently, the intensity of light emission varies every discharge cell,

causing generation of a region where the brightness of emitted light becomes non-uniform on the screen as a whole. The phenomenon of becoming non-uniform in brightness is promoted by the voltage applied to the scan electrode and sustain electrode during the sustain period or by the distortion of wave-forms due to discharge current at the time of sustain discharge.

[0025]

Also, as one of the efforts to enhance the brightness of panels, the partial pressure of xenon (Xe) used as discharge gas is increased, but increasing the brightness in this way will result in making the above-mentioned brightness more non-uniform.

[0026]

Accordingly, in the present invention, with respect to the sustain pulse applied to the scan electrode and sustain electrode during the sustain period, the rise time is shortened on a cycle of once every plurality of times, thereby suppressing the variation of generation timing every discharge cell at the time of sustain discharge. One of the examples is shown in Fig. 5 and Fig. 6.

[0027]

Fig. 5 (a), (b) and Fig. 6 (a), (b) are the enlarged views of essential portions of the sustain pulse applied to the scan electrode and sustain electrode during the sustain period as in Fig. 4. Fig. 5 (a) and Fig. 6 (a) show the sustain pulse applied to the scan electrode, while Fig. 5 (b) and Fig. 6 (b) show the sustain pulse applied to the sustain electrode. Also, the example of Fig. 5, as shown by X, is an example of changing in same timing

the rise time of sustain pulse applied to the scan electrode and sustain electrode, and Fig. 6 is an example of shifting the timing as shown by Y. In Fig. 5 and Fig. 6, A is a period having normal rise time, which is set to about 550ns, and B is a period being shorter in rise time as compared with A, which is set to about 400ns in the present invention.

[0028]

In the present invention, as shown in Fig. 5 and Fig. 6, as for the sustain pulse applied to the scan electrode and sustain electrode during the sustain period, the rise time is shortened on a cycle of at least once every three times, and it is possible to suppress the variation of generation timing of discharge every discharge cell at the time of sustain discharge. Also, the method of shortening the rise time of sustain pulse in this way can be easily realized by changing the inductance of power recovery circuits installed in the scan electrode drive circuit and sustain electrode drive circuit.

[Industrial Applicability]

[0029]

The method for driving a plasma display panel of the present invention is capable of preventing the deterioration of display quality due to non-uniform brightness without increasing the power consumed, and the invention is useful for an image display device using a plasma display panel.

[Brief Description of the Drawings]

[0030]

Fig. 1 is a perspective view showing an essential portion of a panel used in the preferred embodiment of the present invention.

Fig. 2 is an electrode layout of the panel used in the preferred

embodiment.

Fig. 3 is a structural diagram of a plasma display device using the panel driving method in the preferred embodiment of the present invention.

Fig. 4 is a chart of driving voltage wave-forms applied to each electrode of the panel in the preferred embodiment of the present invention.

Fig. 5 is a wave-form diagram showing an example of sustain pulse in the present invention.

Fig. 6 is a wave-form diagram showing another example of sustain pulse in the present invention.

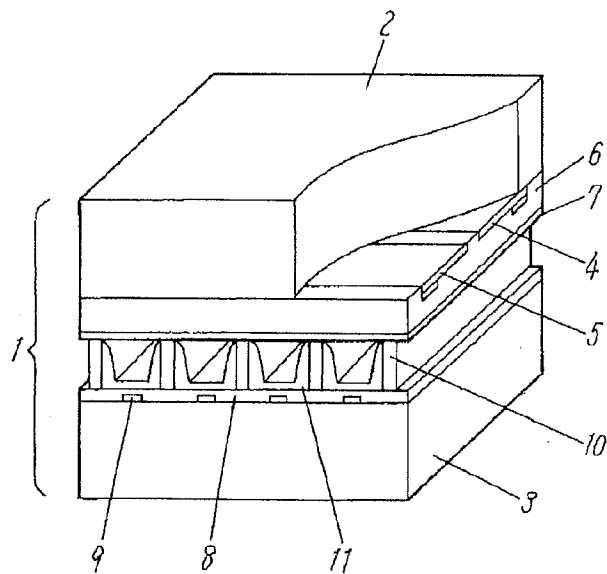
[Description of the Reference Numerals and Signs]

[0031]

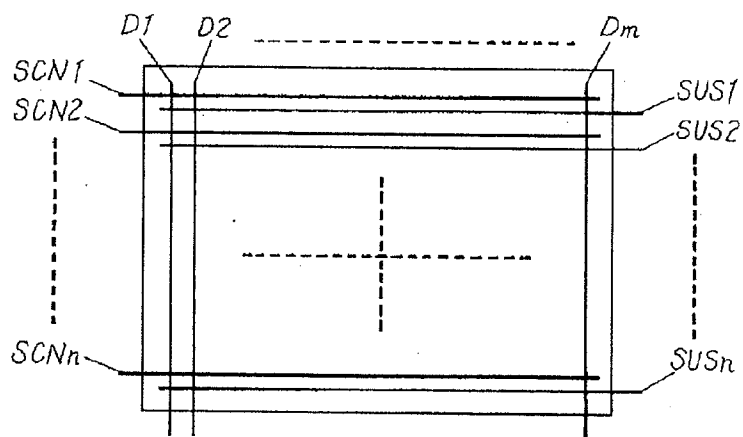
- | | |
|----|---------------------------------|
| 1 | Plasma display panel |
| 2 | Front substrate |
| 3 | Rear substrate |
| 4 | Scan electrode |
| 5 | Sustain electrode |
| 9 | Data electrode |
| 13 | Scan electrode drive circuit |
| 14 | Sustain electrode drive circuit |

[Name of the Document] Drawing

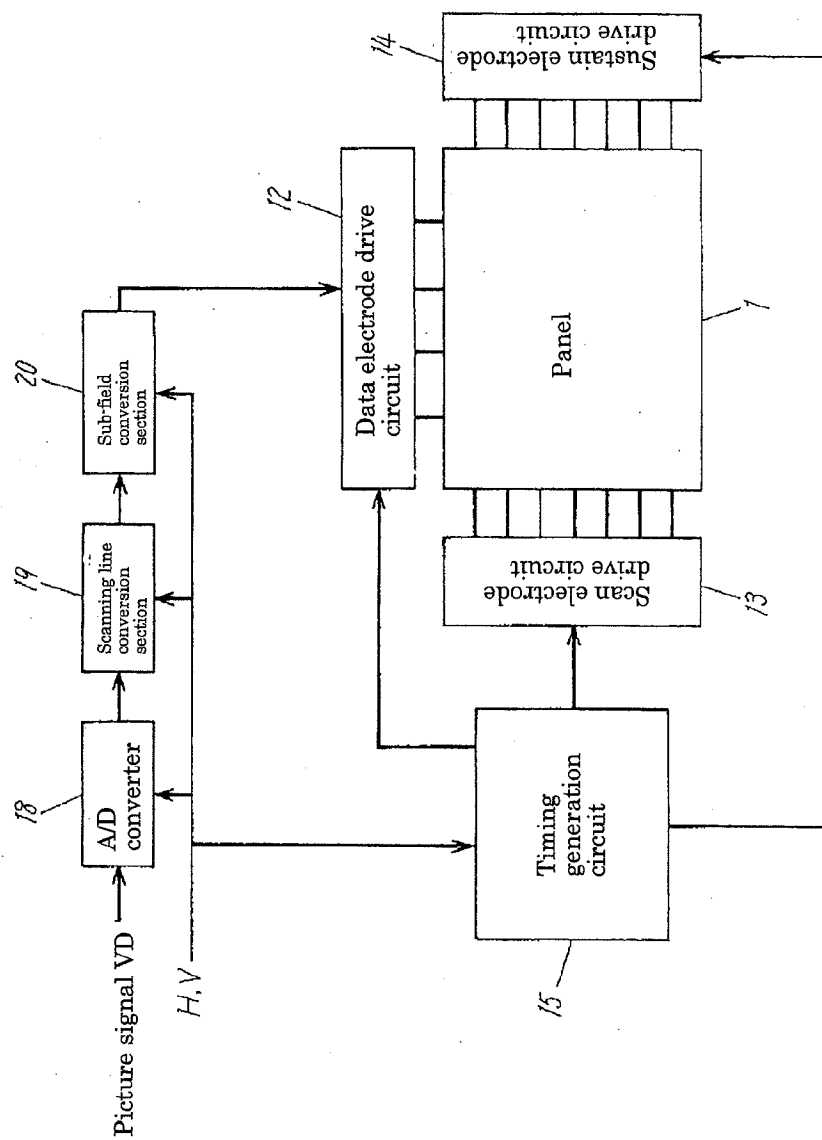
[Fig. 1]



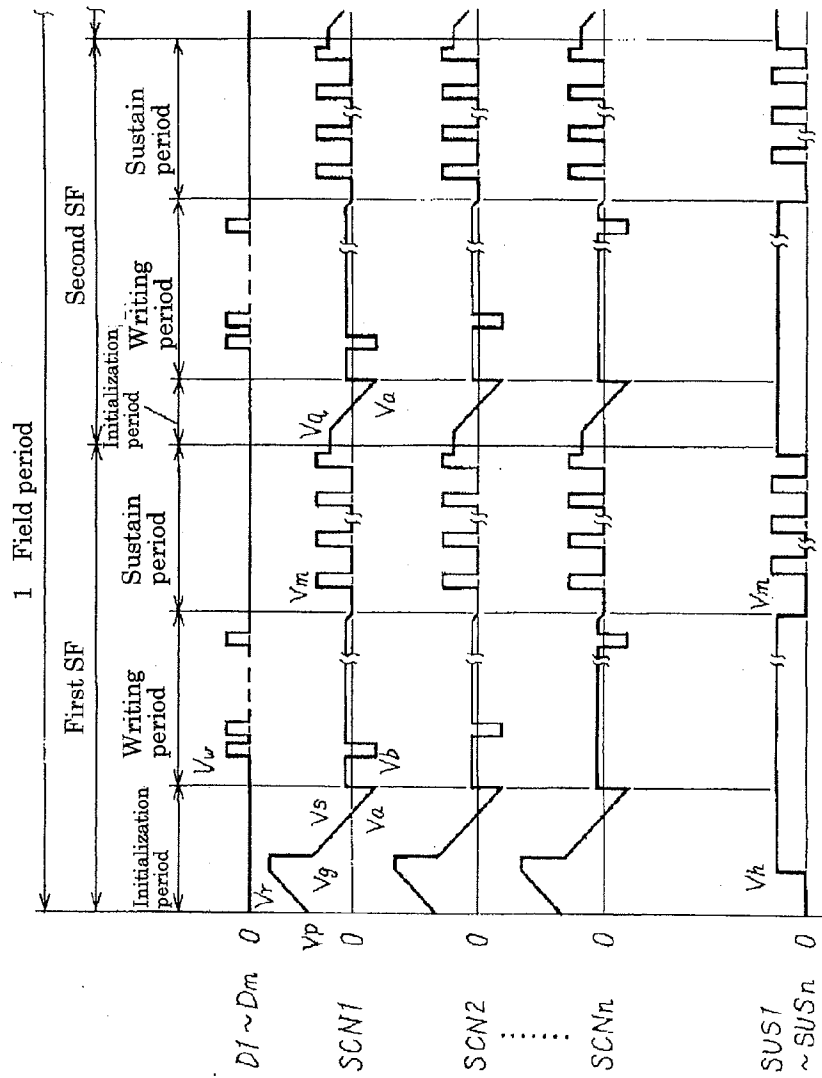
[Fig. 2]



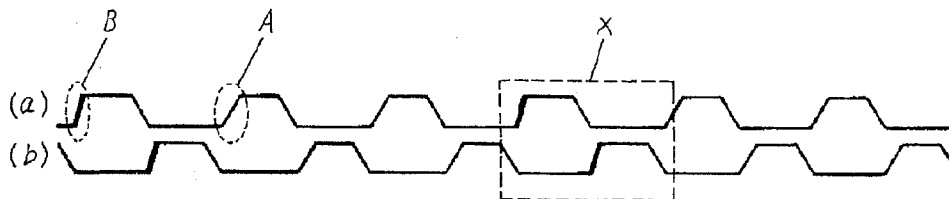
[Fig. 3]



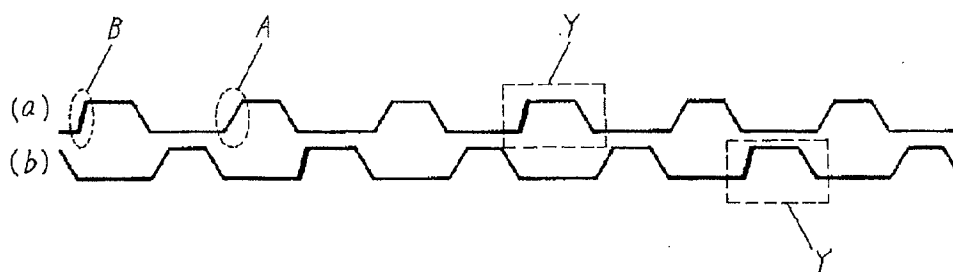
[Fig. 4]



[Fig. 5]



[Fig. 6]



[Name of the Document] Abstract

[Abstract]

[Object] The object of the invention is to prevent the deterioration of display quality due to non-uniform brightness without increasing the power consumed.

[Means to Solve the Problems] A method for driving a plasma display panel having an initialization period in which a discharge cell is formed at an intersection between a scan electrode, a sustain electrode and data electrode, and initializing discharge is generated in the discharge cell, a writing period in which writing discharge is generated in the discharge cell, and a sustain period in which sustain discharge is generated by alternately applying sustain pulses to the scan electrode and the sustain electrode of the discharge cell, wherein the rise time of the sustain pulse applied to the scan electrode and the sustain electrode during the sustain period is shortened on a cycle of once every plurality of times. In this way, it is possible to suppress the variation of generation timing of discharge every discharge cell at the time sustain discharge and to prevent the deterioration of display quality due to non-uniform brightness.

[Selected Drawing] Fig. 5